REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 12/04/06, Applicant is submitting the following argument in response to the Examiner's rejections to the pending claims.

In the Office Action mailed 12/04/06, the Examiner has rejected claims 21, 23-25, 27 and 28 under 35 U.S.C. §103(a) as being unpatentable over Avnon et al. (U.S. Patent 5,559,977; "Avnon") in view of Computer Architecture: A Quantitative Approach by Patterson and Hennessy (noted as "Hennessy" in the last office action). The Examiner has also rejected claims 22 and 26 under 35 U.S.C. §103(a) as being unpatentable over Avnon and Hennessy and further in view of Halfhill ("SiByte Reveals 64-Bit Core for NPUs"). Applicant has considered the reasons noted by the Examiner for the rejections and responds as follows.

In reference to the recitation of the text of the independent claims 21 and 25 that pertain to inhibiting the co-issuance of the second floating point instruction when the first floating point instruction is not a short latency floating point instruction, but not inhibiting the second floating point instruction when the first floating point instruction is a short latency instruction, the Examiner responds by stating that Avnon discloses that subsequent floating point instructions are also inhibited from co-issuance when the first floating point instruction is an "unsafe" floating point instruction. The Examiner further states that a safe floating point instruction is a short latency floating point instruction since it has been determined to be not an exception causing floating point instruction. The Examiner also infers that an unsafe floating point instruction is not a short latency floating point instruction since it can cause an exception, which will have longer latency to handle than the safe floating point instructions.

Applicant submits that the Avnon does not disclose a distinction on latency for floating point instructions. That is, Avnon does not disclose a floating point instruction having short latency versus a floating point instruction that does not have a short latency. The distinction noted by the Examiner pertains to floating point instructions that are safe or unsafe. As noted by the Examiner, a safe instruction is an instruction that has been

determined not to cause an exception. As such, Applicant submits that safe and unsafe floating point instructions are not the same as the short latency and long latency (e.g. not short latency) floating point instructions recited in the amended claims.

Applicant further submits that the amended claims now clearly recite that both the short and long latency floating point instructions generate exceptions to further distinguish the claimed short latency floating point instruction from the safe floating point instruction of Avnon.

Accordingly, for the reasons noted above, Applicant submits that the amended claims overcome the rejections based on Avnon, Hennessy and Halfhill, singly or combined, and respectfully requests the Examiner to withdraw the 35 U.S.C. §103(a) rejections. Hence, Applicant solicits for the allowance of pending claims 21, 22, 24-26 and 28, as amended.

Furthermore, in order to respond to the outstanding office action, Applicant is also submitting a petition for one-month extension of time under a separate cover.

Additionally, please be advised that an IDS was mailed on 03/21/2007 to submit art cited in a counterpart foreign application.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

GARLICK, HARRISON & MARKISON
(Customer No. 51472)

Date: 4-4-2007

By: William W. Kidd

William W. Kidd
Reg. No. 31,772
Phone: (512) 263-1842
Fax No: (512) 263-1469
Email:wkidd@texaspatents.com